



**FOR IMMEDIATE RELEASE**

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**Ambric Increases Productivity in the Programming of Massively Parallel Processors With New Release of aDesigner Tool Suite**

*aDesigner Adds Performance Analysis Capabilities to Optimize Program Execution Across Hundreds of Processors*

**Beaverton, Ore.**, – March 31, 2008 – Ambric<sup>®</sup>, Inc., a fabless semiconductor company delivering the world's first TeraOPS-class of highly scalable, massively parallel processor array (MPPA) devices, announced that it has released a new version of its aDesigner<sup>™</sup> software development tool suite. The new Ambric aDesigner is a comprehensive, easy-to-use tool suite that uses Ambric's award-winning\* structured object programming model (SOPM) to make software development practical for embedded application developers facing the challenges of programming massively parallel processor-based systems. Now with the added performance analysis capabilities, aDesigner enables the optimization of program execution across hundreds of processors, a feature that greatly enhances programming productivity.

**Ambric will be demonstrating aDesigner at Multicore EXPO** in Santa Clara, April 1-2 in booth 23, **at NAB** in Las Vegas, April 14-17 in booth SU13213, **and at ESC** in San Jose, April 15 -17 in booth 1910.

"Today's HD video codec complexity has placed extreme computational requirements on hardware implementations," said Shawn Carnahan, CTO, Telestream. "These codecs challenge even state-of-the-art DSPs and FPGAs and make it very challenging for companies like Telestream to decrease time-to-market and meet form-factor and cost requirements with traditional silicon. When we discovered Ambric's Am2000 massively parallel processor family, with its TeraOPS-class performance, we knew we had found a solution that would answer our

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needs. The aDesigner software development tools are elegant and intuitive—so much so, that designers are getting our implementations done in half the time. Our engineers are even having fun using the tools! Ambric is certainly providing us with what we need to stay competitive, even with the HD challenges of today.”

With aDesigner, it is possible to program hundreds of processors on a single chip. Prior to this, programming tools only provided the capability to program a handful of cores. Furthermore, synchronizing communication among cores or processors was left up to the individual programmer’s ingenuity. This is a daunting task that includes debugging, testing, and optimizing the inter-processor communication and shared memory between cores or processors so as to meet chip-level timing constraints. The aDesigner suite addresses this by offering a single integrated development environment (IDE) for seamless programming across hundreds of processors, leveraging channel communication built into the Am2000 MPPA and enabling users to synchronize debugging across all processors. This greatly reduces program development time, thereby accelerating time-to-market.

### **New Performance Analysis Capabilities Deliver a Significant Productivity Boost**

The new aDesigner enables a significant productivity boost by allowing users to optimize and tune their designs during both simulation and real-time hardware execution. Users can view processor and channel bandwidth utilization in hardware without impacting real-time performance of the design. This is a very powerful and useful capability for optimizing, debugging, and performance tuning the design. aDesigner gives users the ability to view the design at all levels—chip, multi-processor, and individual processor—by using the on-chip dedicated debug network built around every Am2000™ MPPA. Also, users can identify hot and cold spots within the design—processors with high and low utilization—which facilitates design load balance. This capability improves overall throughput.

In addition, users can target code inside a single processor, tweak the code to increase the performance of that processor, and then assess the impact of that change across the group of interconnected processors, as well as the complete Am2000 MPPA device. And users have the ability to measure and analyze activity between any two events across hundreds of processors so as to improve latency. Users can also identify and address data bursts within streaming data so that design performance can be readily improved.

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“We are very pleased with the response we are seeing to our aDesigner tool suite and the productivity gains that our users are experiencing,” said Howard Bubb, Ambric chairman and CEO. “The new aDesigner, with the added performance analysis capability, provides an elegant solution to the real challenge that multicore and MPPA devices present—how to efficiently and productively program multiple cores or processors on a single piece of silicon.”

### **About aDesigner Tool Suite**

The aDesigner tool suite’s powerful graphical user interface (GUI) serves as a cockpit for the user to program the Am2000 MPPA. The design creation, simulation, compilation, realization, and debugging tools, which are included in the tool suite, enable easy creation, verification, and real time execution of the objects that collectively form the complete design. The aDesigner IDE uses the widely-deployed Eclipse framework, a mature and familiar platform, to accelerate developers’ migration. The built-in simulator provides cycle-accurate behavior of the design, and the compiler has a unique optimization capability that takes into account user-defined constraints at both local and global levels. The realization tool enables mapping of the design on single or multiple devices. And the debugger enables bugs to be detected during design simulation and design execution in the real-time hardware system. Together all these tools work seamlessly within aDesigner.

A deterministic and practical approach to system design and programming is possible through the Ambric SOPM, a patented technology that the Am2000 family architecture was built around. The Am2000 architecture was created by first considering the needs of developers in a MPPA environment and then creating a hardware architecture to support those needs. This has resulted in a tight coupling of the programming model and the silicon architecture so that customers can develop applications in weeks, as compared to months with conventional tools. aDesigner also slashes development time because hierarchical objects can be created and then reused to easily build complex objects in software and on the Am2000 MPPA. These objects can be encapsulated and replicated on the same MPPA, as well as across multiple MPPAs. Executing these objects then becomes a simple task as each object is self-contained and control free so there is no global timing closure issue to deal with.

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## **Availability and Pricing**

The new aDesigner software development tool suite is available today. List price starts at \$1,495.00 U.S. For more information about aDesigner, contact Ambric at [sales@ambric.com](mailto:sales@ambric.com).

## **About Ambric, Inc.**

Ambric is a fabless semiconductor company that is shipping the world's first TeraOPS-class device and software development tools that make massively parallel software programming practical for complex embedded systems. The company's highly scalable, massively parallel processor arrays (MPPAs) deliver performance that is more than an order of magnitude greater than high-end digital signal processors (DSPs) and provides a programming model that is much easier than what is available for multiple-DSP platforms. The price-performance exceeds that of field-programmable gate arrays (FPGAs) for complex applications, while enabling faster, easier development in software. Ambric products help companies accelerate time-to-market for their solutions while slashing their system development costs.

Established in 2003 and headquartered in Beaverton, Ore., Ambric has received funding from ComVentures, OVP Venture Partners, Northwest Technology Ventures, and private investors. Visit <http://www.ambric.com> for the latest news and information on the company.

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### **Editor Notes:**

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*\*Ambric was given In-Stat's 2006 Microprocessor Report Analysts' Choice Award for Innovation in February 2007 for its Am2000 family architecture.*

*Photos of the Am2045 MPPA device and a graphic of the new aDesigner tool suite are available from Ambric. Contact Jean Armstrong at [jean@akipr.com](mailto:jean@akipr.com).*