

## Embedded Products Portfolio Brief

### Am2000™ Family

#### Massively Parallel Processing Arrays

#### Applications

- Embedded high-performance applications that normally require multiple high-end DSPs, MPUs, or FPGAs
- Video processing such as codecs, transcoding, transrating filtering, scaling, de-interlacing, de-noising, interpolation, security, or video editing acceleration
- Other processing-intensive applications such as medical imaging, machine vision, image-enhancement, baseband processing, FEC, voice, radar, soft radio, crypto, or test & measurement

#### Benefits

- Create breakthroughs for your toughest application challenges.
- 5-20X performance advantage over high-end 90nm DSPs.
- Up to 4X price-performance over high-end 65nm FPGAs for complex 8/16/32-bit applications.
- Fast time-to-market for your projects.
- Reduced complexity and cost of development vs. high-end FPGAs or DSPs.
- Reduced cost, power and footprint vs. multi-chip DSP/FPGA-based systems.
- Enables profitable customer-specific enhancements.
- Productive tool suite.
- Fully or partially field-programmable, in milliseconds.
- Object re-use far exceeds re-use of RTL or DSP libraries.
- Use existing software library objects and easily integrate with proprietary objects you create.

### Am2000 Family Features

#### Breakthrough MIMD Parallel Programming Model

- Practical and intuitive, the structural object programming model tames data and control complexity.

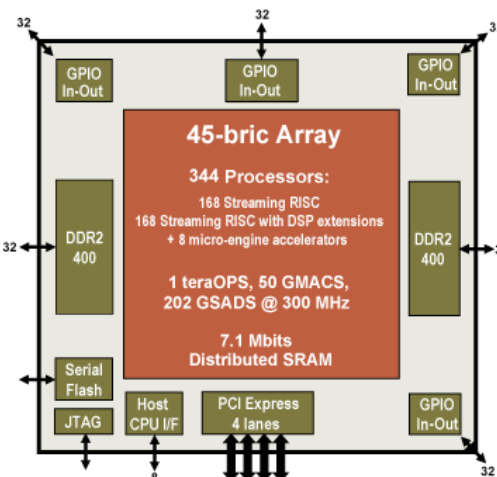
#### Asynchronous, Scalable, Massively-Parallel MIMD Array

- The Am2045 has 336 fixed-point, 32-bit RISC processors containing 672 ALUs, in a tiled array of 42 brics.

#### Reconfigurable

- Configuration via PCI Express, host interface, serial Flash, or JTAG

Number of brics	# of RISC	# of peng	Mbits SRAM	tera OPS	GMACS 16x16-32-bit	Est. Watts
Am2045	336	8	7.14	1.03	50	6-16
Am2029	216	4	4.55	0.66	32	4-11
Am2016	120	0	2.46	0.36	18	4-6



Am2000 teraOPS-Class Chip Diagram

#### Up to 7.1 Mbits Distributed Memory

- Eight 2-KByte SRAM blocks per bric, plus dedicated memory for each processor, for data or instructions..

#### Inherently Energy-Efficient

- Up to 87 clock domains for performance-power tradeoffs under software control — from 300 MHz down to 0.15 MHz. Synchronization across domains is automatic in hardware.
- Asynchronous fabric eliminates both high-speed global interconnect and complex system-level state-machines.

#### Robust External I/O

- One built-in PCI Express® end-point: 4 lanes, 2.5 Gbps/lane. Can be used to configure Am2000 chips.
- Up to two discrete 16-bit DDR2-400 devices per 32-bit I/F for 3.2 GBytes/s peak bandwidth and 1 Gbyte capacity.
- Aggregate GPIO bandwidth: up to 128-bits, ~ 13 Gbps.
- Up to 4 32-bit GPIOs. Each can be partitioned into 16-bit, single-bit, or multi-bit uses. Each can be set for input or output
- GPIO supports glueless connection to HD-SDI and DVB-ASI SERDES chips, ADCs, DACs, FPGAs, sensors, etc.

#### Globally Asynchronous On-chip Interconnect

- Asynchronous messaging channels are a fundamental invention that enable both the breakthrough programming model and practical debugging for a massively-parallel array.

**aDesigner™ comprehensive tool suite for Am2000™ Family Structured Object Programming**

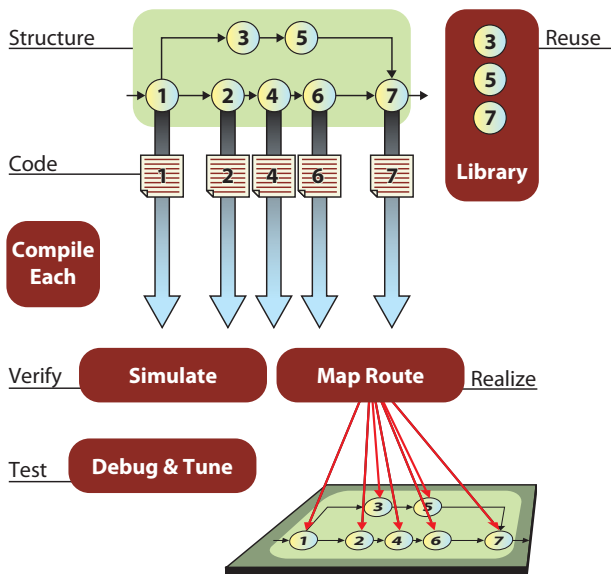
aDesigner is the first practical software development tool suite for programming Massively Parallel Processor Array platforms. It is a comprehensive, easy-to-use tool suite that uses Ambric’s award-winning\* structured object programming model (SOPM) to make software development practical for embedded application developers who need to harness the power of massively parallel processor-based systems.

**The Ambric Programming Model**

The following table summarizes Ambric’s Structural Object Programming (SOP) model:

<b>Structure</b>	Describe the design as a structure of objects and their associated control/data-flow.
<b>Code</b>	Implement objects in Java or assembly language.
<b>Reuse</b>	Take advantage of validated library objects for common functions.
<b>Verify</b>	Verify the implementation using the simulator.
<b>Realize</b>	Map the design to the target Ambric device with the mapping & routing tool.

**Flow of Development:**



For more information, contact Ambric sales at (503) 601-6500 or email sales@ambric.com

**Am2045™ Integrated Development Board**



**Features**

- One Am2045™ Massively Parallel Processor Array
- Single slot 4-lane PCIe interface
- USB 2.0 interface
- FPGA for GPIO control

**Benefits**

- Speed software development by executing, debugging and performance-tuning your code directly on the Am2045 device.
- Tight integration with aDesigner™ Tool Suite
- Ability to configure the Am2045 through multiple interfaces – Flash, PCIe or USB
- Direct interface to another Am2045 device or developer’s prototype board through external high-speed connectors

**Am2045 GT™ Development and Accelerator Board**



**Features**

- One Am2045™ Massively Parallel Processor Array
- Single slot 4-lane PCIe interface
- Standard single slot clearance, 2.7” x 5” board size and low profile fan
- Development on Windows platform

**Benefits**

- Speed software development by executing, debugging and performance-tuning your code directly on the Am2045 device
- Accelerator board for boosting performance of new and current applications
- Tight integration with aDesigner™ Tool Suite
- Compact form factor enables installation on any standard system with PCIe slot